CLAIMS

What is claimed is:

1. A method for placing circuit elements on an integrated circuit comprising:

a) placing cells of a first circuit design by use of non-direct timing driven techniques, wherein said placing produces a first placement; and

b) placing said cells by use of direct timing driven placement techniques, wherein said first placement is an input into said placing.

2. The method of Claim 1 wherein said a) comprises:

a1) placing cells of a first circuit design to minimize total weighted length of wiring interconnecting said cells, wherein said placing produces a first placement.

3. A method for placing circuit elements on an integrated circuit comprising:

a) placing cells of a first circuit design by use of non-direct timing driven techniques, wherein said placing produces a first placement;

b) routing said wiring to connect said cells, wherein said routing produces a first layout;

c) modifying said first circuit design to produce second cells of a second circuit design; and

d) placing said second cells by use of direct timing driven placement techniques.

4. The method of Claim 3 wherein said a) comprises:

a1) placing cells of a first circuit design to minimize total weighted length of wiring interconnecting said cells, wherein said placing produces a first placement.

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5. The method of Claim 3 wherein said b) comprises:

b1) estimating congestion for wiring to connect said cells, wherein said first placement is further a first layout.

10 6. The method of Claim 3 wherein said c) comprises:

c1) modifying said first circuit design to achieve minimum required signal timing within said first layout, wherein said modifying produces a second circuit design containing second cells.

15 7. The method of Claim 3 wherein said c) comprises:

c1) modifying said first circuit design to enlarge cell area allocations within congested regions of said first layout, wherein said modifying produces a second circuit design containing second cells.

20 8. A method for placing circuit elements on an integrated circuit comprising:

a) placing cells of a first circuit design by use of non-direct timing driven techniques, wherein said placing produces a first placement;

b) routing said wiring to connect said cells, wherein said routing produces a first layout;

c) placing said cells by use of direct timing driven placement techniques to produce a new placement, wherein said first layout is an input into said placing;

d) routing said new placement, wherein said routing produces a new layout; and

e) placing said cells by use of direct timing driven placement techniques to produce still another new placement, wherein said new layout is an input into said placing.

9. The method of Claim 8 wherein said a) comprises:

a1) placing cells of a first circuit design to minimize total weighted length of wiring interconnecting said cells, wherein said placing produces a first placement.

10. The method of Claim 8 wherein said b) comprises:

b1) estimating congestion for wiring to connect said cells, wherein said first placement is further a first layout.

11. The method of Claim 8 wherein said d) and e) are repeated.

12. A method for placing circuit elements on an integrated circuit comprising:

a) synthesizing a high level description of a circuit to produce a first circuit design;

b) placing cells of a first circuit design by use of non-direct timing driven techniques, wherein said placing produces a first placement;

c) routing said wiring to connect said cells, wherein said routing produces a first layout;

d) modifying said first circuit design to produce a second high level description of a circuit;

e) synthesizing said second high level description of a circuit to produce a second circuit design; and

f) placing second cells of said second circuit design by use of direct timing driven placement techniques.

13. The method of Claim 12 wherein said b) comprises:

b1) placing cells of a first circuit design to minimize total weighted length of wiring interconnecting said cells, wherein said placing produces a first placement.

14. The method of Claim 12 wherein said c) comprises:

c1) estimating congestion for wiring to connect said cells, wherein said first placement is further a first layout.

15.The method of Claim 12 wherein said c), e) and f) are repeated.

16. The method of Claim 12 wherein said c), d), e) and f) are repeated.

17. The method of Claim 12 wherein said d) comprises:

d1) modifying said first circuit design to achieve minimum required signal timing within said first layout, wherein said modifying produces a second circuit design containing second cells.

18. The method of Claim 12 wherein said d) comprises:

d1) modifying said first circuit design to enlarge cell area allocations within congested regions of said first layout, wherein said modifying produces a second circuit design containing second cells.

19. A system comprising:

a processor coupled to a bus;

a memory coupled to said bus and wherein said memory contains instructions that when executed implement a method for placing circuit elements on an integrated circuit, said method comprising the steps of:

a) placing cells of a first circuit design without regard to circuit timing, wherein said placing produces a first placement; and

b) placing said cells by use of direct timing driven placement techniques, wherein said first placement is an input into said placing.

20. A system as described in Claim 19 wherein said a) comprises:

a1) placing cells of a first circuit design to minimize total weighted length of wiring interconnecting said cells, wherein said placing produces a first placement.